REMARKS

Claims 22 and 24-37 are pending in the present application. In the Office Action dated January 19, 2001, the Examiner (1) rejected claims 26-31 and 34 under 35 USC § 102(b) as being anticipated by Kimura et al. (US 5,583,358); (2) rejected claim 34 under 35 USC § 102(b) as being anticipated by Shimbo (US 4,980,306); (3) rejected claims 22, 24, 25, 32, 35, and 37 under 35 USC § 102(b) as being anticipated by Morita et al. (US 5,073,813); (4) rejected claims 22 and 25-36 under 35 USC § 102(b) as being anticipated by Manning et al. (US 5,411,909); (5) rejected claim 33 under 35 USC § 103(a) as being unpatentable over Morita *et al.* (US 5,073,813); and (6) rejected claims 24 and 37 under 35 USC § 103(a) as being unpatentable over Manning et al. (US 5,411,909).

Applicants respectfully request reconsideration of claims 22 and 24-37 in view of the foregoing amendments and the following remarks. Some of the technical differences between the applied references and embodiments of the invention will now be discussed. Of course, these discussed differences regarding the embodiments, which are disclosed in detail in the patent specification, do not define the scope or interpretation of any of the claims. Where presented below, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Generally, the disclosed embodiments are directed to methods and apparatus having trench isolation structures with reduced isolation pad heights and reduced edge spacers. In one embodiment, an microelectronic device comprises a microelectronic substrate, a gate structure including a gate oxide layer formed on the substrate, a first gate layer formed on the gate oxide layer, and an adhesion layer formed on the first gate layer. The gate structure has a trench at least partially disposed therein and extending into the substrate, and a field oxide layer is at least partially in the trench. The field oxide layer has substantially straight sides not contacting the gate oxide layer and extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

In an alternate embodiment, Applicants teach a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, and a field oxide in the trench. The field oxide has substantially straight sides projecting outwardly from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate. A component is formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

The microelectronic structures taught by Applicants provide several advantages over prior art structures. Because the height of the field oxide "isolation pad" is reduced compared with the height of the gate structure, edge spacers that may otherwise form along the edges of the isolation pad are reduced or eliminated. Therefore, the isolation pad advantageously requires less surface area on the apparatus.

Furthermore, because the field oxide has substantially straight sides projecting outwardly from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate, the field oxide isolation pad occupies less space on the substrate which is critical to the design of highly integrated microelectronics devices. Isolation pad structures that project outwardly from the trench may also provide improved isolation characteristics between adjacent components formed on the substrate and components formed on the isolation pad.

Kimura et al.

Kimura et al. (U.S. 5,583,358) teaches a semiconductor memory device having stacked capacitors. According to the teachings of Kimura et al., the memory device includes an isolating film 12 that fills a trench within an Si substrate 11, and also extends laterally over the surface of the Si substrate 11 (Figures 18a-c). The isolating film 12 of Kimura et al. does not project upwardly from the trench with straight sides, and there is no discontinuity between the isolating film 12 and the surrounding surface level. As best shown in Figure 18c, there is no edge of the isolating film 12 upon which an edge spacer 32 may form.

Kimura et al. does not disclose, teach or fairly suggest the microelectronics structures as taught by Applicants. Specifically, Kimura et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides*

and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate*, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. As best shown in Applicants' Figure 2H, the microelectronics structures taught by Applicants include a field oxide isolation pad that has straight sides that extend upwardly from the trench to form a raised isolation pad. Isolation pad structures that project outwardly from the trench may advantageously provide improved isolation characteristics between adjacent components formed on the substrate and components formed on the isolation pad. Such structures may also occupy less surface area on the microelectronics device. Thus, Kimura et al. does not disclose, teach or fairly suggest microelectronics structures taught by Applicants.

Shimbo

Shimbo (U.S. 4,980,306) teaches a semiconductor device having an isolation trench 30 formed within a p-type substrate 1 between a pair of adjacent transistors 100, 200. A p-type selective epitaxial film 20 is formed on the sidewalls and bottom of the trench 30. A silicon dioxide 17 is formed within the trench 30 on the p-type epitaxial film 20. As shown in Figure 2c of Shimbo, the silicon dioxide 17 projects laterally from the trench 30 over surrounding portions of the p-type film 20. As shown in Figure 2e, the silicon dioxide 17 projects upwardly from the trench 30 to a height that is greater than the first gate layers 104, 204 of the adjacent transistors 100, 200.

Shimbo does not disclose, teach or fairly suggest the microelectronics structures as taught by Applicants. Specifically, Shimbo does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate*. As described above, Shimbo teaches that the field oxide layer (silicon dioxide) projects laterally from the trench 30, and not straight up from the trench. As a result, the microelectronics structures taught by Applicants may have field oxide layers that occupy less area on the surface of the substrate, and may provide improved isolation characteristics over those taught by Shimbo.

Shimbo also does not disclose, teach or fairly suggest the microelectronics structures including a field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. Shimbo teaches that the field oxide level is greater than the level of the upper surface of the first gate layer of the adjacent transistors 100, 200. As a result, in the microelectronics structures taught by Applicants, there is less edge of the field oxide layer for edge spacers to form. Thus, Shimbo does not disclose, teach or fairly suggest microelectronics structures taught by Applicants.

Morita et al.

Morita et al. (U.S. 5,073,813) teaches semiconductor devices having a groove 37 formed in a silicon substrate 31. An oxide film 38 is formed over the sides and bottom of the groove 37 and an oxide film 34 extends laterally over the surface of the substrate 31, as shown in Figure 2F of Morita et al.. (4:31-32; 4:10-11). A second insulating oxide 40 is formed within the groove 37 on the oxide film 38. First and second gate electrodes 36a, 41a are formed by etching. As best shown in Figure 2J, the resulting isolation structure taught by Morita et al. includes a field oxide that extends upwardly from the groove (portions 38 and 40) and also extends laterally from the groove over the surface of the substrate 31 (portions 32 shown on either side of the groove).

Morita et al. does not disclose, teach or fairly suggest the microelectronics structures as taught by Applicants. Specifically, Morita et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate.* Thus, Morita et al. does not disclose, teach or fairly suggest microelectronics structures taught by Applicants. As described above, according to Morita et al., the field oxide extends laterally over the surface of the substrate.

Manning et al.

Manning et al. (U.S. 5,411,909) teaches semiconductor devices having a field isolation region 104 recessed within a substrate 102. Manning et al. teaches that the field

isolation region 104 is preferably "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar." (6:38-41). As best shown in Figure 11 of Manning et al., the field isolation region 104 has non-straight sides that do not extend upwardly from the trench above the substrate 102.

Manning et al. does not disclose, teach or fairly suggest the microelectronics structures as taught by Applicants. Specifically, Manning et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate*, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. According to Manning et al., the field isolation region 104 has non-straight sides that do not extend upwardly from the trench above the substrate 102.

In fact, Manning et al. teaches away from the microelectronics structures taught by Applicants. Because Manning et al. teaches that the field isolation region 104 should be "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar," Manning et al. teaches away from Applicants' invention. According to the teachings of Applicants, the field oxide layer has a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Manning

Manning (U.S. 5,177,028) teaches microelectronic devices including a trench 108 formed in a substrate 102. As best shown in Figure 13, a field oxide layer 112 is formed within the trench 108 and a pad oxide layer 104 is formed on the substrate 102 in contact with the field oxide layer 112. Thus, Manning teaches an isolation structure that extends upwardly from the trench 108 (field oxide layer 112) and that also extends laterally over the surface of the substrate 102 (pad oxide layer 104).

Manning does not disclose, teach or fairly suggest the microelectronics structures as taught by Applicants. Specifically, Manning does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides*

and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate.* Thus, Manning does not disclose, teach or fairly suggest microelectronics structures taught by Applicants. As described above, according to Manning Manning, the field oxide extends laterally over the surface of the substrate.

I. Rejection of claims 26-31 and 34 under 35 USC § 102(b) as being anticipated by Kimura et al. (US 5,583,358).

Turning now to the specific language of the claims, claim 26 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a field oxide in the trench, *the field oxide having substantially straight sides projecting outwardly from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate*, and a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate. (emphasis added).

Kimura et al. does not disclose, teach or fairly suggest the microelectronics structures as taught by Applicants. Specifically, Kimura et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate*, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. Thus, Kimura et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 26.

Similarly, claim 28 recites microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a field oxide in the trench, *the field oxide having substantially straight sides extending from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate*, and a gate structure formed on the substrate, the gate structure extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure. (emphasis added)

Kimura et al. does not disclose, teach or fairly suggest the microelectronics structures recited in claim 28. Specifically, Kimura et al. does not teach or suggest microelectronics structures including a field oxide having substantially straight sides extending from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate. Thus, Kimura et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 28.

Claim 30 recites a microelectronic device, comprising a microelectronic substrate having a recess formed in a surface thereof, and a field oxide deposited in the recess, *the field oxide having substantially straight sides extending from the recess beyond the surface of the substrate* by a height which is less than or equal to approximately one half of a height of a component formed on the field oxide, *the field oxide not extending laterally from the recess over the surface of the substrate.* (emphasis added).

Kimura et al. does not disclose, teach or fairly suggest the microelectronics structures recited in claim 30. Specifically, Kimura et al. does not teach or suggest microelectronics structures including a field oxide having substantially straight sides and not extending laterally from the trench over the surface of the substrate. Thus, Kimura et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 28.

Also, claim 34 recites a microelectronic device, comprising a microelectronic substrate having a trench formed therein, *a field oxide within the trench and having substantially straight sides projecting therefrom* by a height which is small enough to prevent the formation of spacers adjacent the field oxide, *the field oxide not extending laterally from the trench over the surface of the substrate*, and a component formed on the field oxide. (emphasis added).

Kimura et al. does not disclose, teach or fairly suggest the microelectronics structures recited in claim 34. Specifically, Kimura et al. does not teach or suggest microelectronics structures including a field oxide having substantially straight sides and not extending laterally from the trench over the surface of the substrate. Thus, Kimura et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 34.

Claims 27, 29, and 31 depend from claims 26, 28, and 30 respectively, and are therefore patentable for the same reasons as their respective base claims. For the foregoing

reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 26-31 and 34 under 35 USC § 102(b) as being anticipated by Kimura et al..

II. Rejection of claim 34 under 35 USC § 102(b) as being anticipated by Shimbo (US 4,980,306).

Claim 34 recites a microelectronic device, comprising a microelectronic substrate having a trench formed therein, *a field oxide within the trench and having substantially straight sides projecting therefrom* by a height which is small enough to prevent the formation of spacers adjacent the field oxide, *the field oxide not extending laterally from the trench over the surface of the substrate*, and a component formed on the field oxide. (emphasis added).

Shimbo. does not disclose, teach or fairly suggest the microelectronics structures recited in claim 34. Specifically, Shimbo does not teach or suggest microelectronics structures including a field oxide having substantially straight sides and not extending laterally from the trench over the surface of the substrate. Thus, Shimbo does not disclose, teach or fairly suggest microelectronics structures as recited in claim 34.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 34 under 35 USC § 102(b) as being anticipated by Shimbo.

III. Rejection of claims 22, 24, 25, 32, 35, and 37 under 35 USC § 102(b) as being anticipated by Morita et al. (US 5,073,813).

Claim 22 recites a microelectronic device comprising a microelectronic substrate, a gate structure including a gate oxide layer formed on the substrate, a first gate layer formed on the gate oxide layer, and an adhesion layer formed on the first gate layer, the gate structure having a trench at least partially disposed therein and extending into the substrate, and a field oxide layer at least partially in the trench having substantially straight sides not contacting the gate oxide layer and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate*, the field oxide

layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Morita et al. does not disclose, teach or fairly suggest the microelectronics structures as recited in Applicants' claim 22. Specifically, Morita et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate.* As described above, according to Morita et al., the field oxide extends laterally over the surface of the substrate. Thus, Morita et al. does not anticipate claim 22.

Claims 24, 25, 34, and 37 depend from claim 22 and are therefore patentable over Morita et al. for the same reasons as claim 22 and also due to additional limitations contained in those claims. For example, claim 24 recites the microelectronic device of claim 22, further comprising a silicide layer formed on the adhesion layer. Claim 25 recites the microelectronic device of claim 22, further comprising a conductive layer formed on the adhesion layer. Claim 35 recites the microelectronic device of claim 22 wherein the first gate layer comprises a polysilicon layer. Claim 37 recites the microelectronic device of claim 24 wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the silicide layer. Claims 24, 25, 34, and 37 are therefore also not anticipated by Morita et al..

Claims 32 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, a first gate layer formed on the gate oxide layer, an adhesion layer formed on the first gate layer, and a conductive layer formed on the adhesion layer, and a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, *the field oxide having substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate.* (emphasis added).

Morita et al. does not disclose, teach or fairly suggest the microelectronics structures as recited in Applicants' claim 32. Specifically, Morita et al. does not teach or

suggest microelectronics structures including *the field oxide having substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate.* As described above, according to Morita et al., the field oxide extends laterally over the surface of the substrate. Thus, Morita et al. does not anticipate claim 32.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 22, 24, 25 32, 35, and 37 under 35 USC § 102(b) as being anticipated by Morita et al..

IV. Rejection of claims 22 and 25-36 under 35 USC § 102(b) as being anticipated by Manning et al. (US 5,411,909).

Claim 22 recites a microelectronic device comprising a microelectronic substrate, a gate structure including a gate oxide layer formed on the substrate, a first gate layer formed on the gate oxide layer, and an adhesion layer formed on the first gate layer, the gate structure having a trench at least partially disposed therein and extending into the substrate, and a field oxide layer at least partially in the trench having substantially straight sides not contacting the gate oxide layer and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate,* the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Manning et al. does not disclose, teach or fairly suggest the microelectronics structures as recited in Applicants' claim 22. Specifically, Manning et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate.* As described above, according to Manning et al., the field oxide extends laterally over the surface of the substrate. Thus, Manning et al. does not anticipate claim 22.

Manning et al. teaches away from the microelectronics structures recited in claim 22. Because Manning et al. teaches that the field isolation region 104 should be "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar," Manning et al. teaches away from Applicants'

claim 22, which recites that the field oxide layer has a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Claims 25, 34, and 37 depend from claim 22 and are therefore patentable over Manning et al. for the same reasons as claim 22 and also due to additional limitations contained in those claims. Claim 25 recites the microelectronic device of claim 22, further comprising a conductive layer formed on the adhesion layer. Claim 35 recites the microelectronic device of claim 22 wherein the first gate layer comprises a polysilicon layer. Claim 37 recites the microelectronic device of claim 24 wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the silicide layer. Claims 24, 25, 34, and 37 are therefore also not anticipated by Manning et al..

Claim 26 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a field oxide in the trench, *the field oxide having substantially straight sides projecting outwardly from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate*, and a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate. (emphasis added).

Manning et al. does not disclose, teach or fairly suggest the microelectronics structures as taught by Applicants. Specifically, Manning et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate*, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. Thus, Manning et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 26.

Manning et al. teaches away from the microelectronics structures recited in claim 26. Because Manning et al. teaches that the field isolation region 104 should be "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar," Manning et al. teaches away from Applicants'

claim 26, which recites that the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Similarly, claim 28 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a field oxide in the trench, *the field oxide having substantially straight sides extending from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate*, and a gate structure formed on the substrate, the gate structure extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure. (emphasis added).

Manning et al. does not disclose, teach or fairly suggest the microelectronics structures recited in claim 28. Specifically, Manning et al. does not teach or suggest microelectronics structures including a field oxide having substantially straight sides extending from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate. Thus, Manning et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 28.

Manning et al. teaches away from the microelectronics structures recited in claim 28. Because Manning et al. teaches that the field isolation region 104 should be "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar," Manning et al. teaches away from Applicants' claim 28, which recites that the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Claim 30 recites a microelectronic device, comprising a microelectronic substrate having a recess formed in a surface thereof, and a field oxide deposited in the recess, *the field oxide having substantially straight sides extending from the recess beyond the surface of the substrate* by a height which is less than or equal to approximately one half of a height of a component formed on the field oxide, *the field oxide not extending laterally from the recess over the surface of the substrate.* (emphasis added).

Manning et al. does not disclose, teach or fairly suggest the microelectronics structures recited in claim 30. Specifically, Manning et al. does not teach or suggest microelectronics structures including a field oxide having substantially straight sides and not

extending laterally from the trench over the surface of the substrate. Thus, Manning et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 28.

Also, claim 34 recites a microelectronic device, comprising a microelectronic substrate having a trench formed therein, *a field oxide within the trench and having substantially straight sides projecting therefrom* by a height which is small enough to prevent the formation of spacers adjacent the field oxide, *the field oxide not extending laterally from the trench over the surface of the substrate*, and a component formed on the field oxide. (emphasis added).

Manning et al. does not disclose, teach or fairly suggest the microelectronics structures recited in claim 34. Specifically, Manning et al. does not teach or suggest microelectronics structures including a field oxide having substantially straight sides and not extending laterally from the trench over the surface of the substrate. Thus, Manning et al. does not disclose, teach or fairly suggest microelectronics structures as recited in claim 34.

Manning et al. teaches away from the microelectronics structures recited in claim 34. Because Manning et al. teaches that the field isolation region 104 should be "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar," Manning et al. teaches away from Applicants' claim 34, which recites that a field oxide within the trench and having substantially straight sides projecting therefrom.

Claims 27, 29, 31, and 35-36 depend from claims 26, 28, 30, and 22, respectively, and are therefore patentable for the same reasons as their respective base claims. For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 22 and 25-36 under 35 USC § 102(b) as being anticipated by Manning et al..

V. Rejection of claim 33 under 35 USC § 103(a) as being unpatentable over Morita et al. (US 5,073,813).

Claim 33 depends from claim 32, which recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, a first gate layer formed on the gate oxide layer, an adhesion

layer formed on the first gate layer, and a conductive layer formed on the adhesion layer, and a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, *the field oxide having substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate.* (emphasis added). Claim 33 recites the microelectronic device of claim 32, further comprising an oxide spacer adjacent the gate structure.

Morita et al. does not disclose, teach or fairly suggest the microelectronics structures as recited in Applicants' claim 33. Specifically, Morita et al. does not teach or suggest microelectronics structures including *the field oxide having substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate.* As described above, according to Morita et al., the field oxide extends laterally over the surface of the substrate. Thus, Morita et al. does not render claim 33 unpatentable.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 33 under 35 USC § 103(a) as being unpatentable over Morita et al..

VI. Rejection of claims 24 and 37 under 35 USC § 103(a) as being unpatentable over Manning et al. (US 5,411,909).

Claims 24 and 37 depend from claim 22, which recites a microelectronic device comprising a microelectronic substrate, a gate structure including a gate oxide layer formed on the substrate, a first gate layer formed on the gate oxide layer, and an adhesion layer formed on the first gate layer, the gate structure having a trench at least partially disposed therein and extending into the substrate, and a field oxide layer at least partially in the trench having substantially straight sides not contacting the gate oxide layer and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate*, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. Claim 24 recites the microelectronic device of claim 22, further comprising a silicide layer formed on the adhesion layer. Claim 37 recites the microelectronic device of claim 22 wherein the field

oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the silicide layer.

Manning et al. does not disclose, teach or fairly suggest the microelectronics structures as recited in Applicants' claims 24 and 37. Specifically, Manning et al. does not teach or suggest microelectronics structures including a field oxide layer *having substantially straight sides* and *extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate.* As described above, according to Manning et al., the field oxide extends laterally over the surface of the substrate.

Manning et al. teaches away from the microelectronics structures recited in claim 22. Because Manning et al. teaches that the field isolation region 104 should be "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar," Manning et al. teaches away from Applicants' claim 22, which recites that the field oxide layer has a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Manning et al. teaches away from the microelectronics structures recited in claims 24 and 37. Because Manning et al. teaches that the field isolation region 104 should be "fully recessed within the substrate 102 so that substrate 102 and field isolation region 104 have top surfaces which are substantially coplanar," Manning et al. teaches away from Applicants' claim 24 and 37, which recites that the field oxide layer has a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. Thus, Manning et al. does not render claims 24 and 37 unpatentable.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 24 and 37 under 35 USC § 103(a) as being unpatentable over Manning et al..

CONCLUSION

In light of the foregoing amendments and remarks, Applicants believe that pending claims 22 and 24-37 are in condition for allowance, and that action is respectfully requested. In accordance with 37 CFR § 1.121, attached hereto is an attached page entitled "Version with Markings to Show Changes Made" showing the specific changes made to the

claims by the current amendment. If there are any remaining matters that can be handled in a telephone conference, the Examiner is invited to telephone the undersigned attorney, Dale C. Barr, at (206) 903-8745.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claims 22, 26, 28, 30, 32, and 34 as follows:

22. (Three Times Amended) A microelectronic device, comprising:

a microelectronic substrate;

a gate structure including a gate oxide layer formed on the substrate, a first gate layer formed on the gate oxide layer, and an adhesion layer [composed of a material other than a conductively doped polysilicon material] formed on the first gate layer, the gate structure having a trench at least partially disposed therein and extending into the substrate; and

a field oxide layer at least partially in the trench having substantially straight sides not contacting the gate oxide layer and extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate, the field oxide layer having a field oxide level between the level of the [an] upper surface of the substrate and the level of an upper surface of the first gate layer.

26. (Twice Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide having substantially straight sides projecting outwardly [extending] from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate; and

a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

28. (Twice Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide having substantially straight sides extending from the trench beyond the surface of the substrate and not extending laterally from the trench over the surface of the substrate; and

a gate structure formed on the substrate, the gate structure extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure.

30. (Twice Amended) A microelectronic device, comprising:

a microelectronic substrate having a recess formed in a surface thereof; and

a field oxide deposited in the recess, the field oxide having substantially straight sides extending from the recess beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of a component formed on the field oxide, the field oxide not extending laterally from the recess over the surface of the substrate.

32. (Three Times Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, a first gate layer formed on the gate oxide layer, an adhesion layer [composed of a material other than a conductively doped polysilicon material] formed on the first gate layer, and a conductive layer formed on the adhesion layer; and

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, the field oxide having substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate.

34. (Twice Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed therein;[,]

a field oxide within the trench and having substantially straight sides projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide, the field oxide not extending laterally from the trench over the surface of the substrate; and

a component formed on the field oxide.